ADAPTER FOR TRANSMISSION LINES USING HDLC FRAMES

Related Application

An application entitled "System for Providing Simultaneous Multiple Circuit-Switched Type Communications on an ISDN Basic Rate Interface" has been filed for Chi-Chang Chen, Bor-shen Wu, Jen-Yung Lin, and Min-Chang Lin on May 14, 1992 and bears Serial No. 07/882,784. This application contains subject matter related to the subject matter of the present application and is incorporated herein by reference.

Field of the Invention

The present invention relates to an adapter for use in a telecommunications network. The adapter connects a first transmission line with a low bit rate and a second transmission line with a higher bit rate. Preferably both the first and second transmission lines use a High Level Data Link Control (HDLC) type protocol. The invention is especially useful in an ISDN network.

Background of the Invention

The High Level Data Link Control protocol was developed by the International Standards Organization (ISO). The HDLC protocol is a data link control protocol used in various networks such as ISDN (Integrated Services Digital Network). The HDLC protocol uses synchronous transmission. All

transmissions are in frames. A single frame format suffices for all types of data and control exchanges.

FIG 1 illustrates a conventional HDLC frame. The frame has the following fields:

Flag (F)	- 8 bits
Address (A)	- One or more octets (i.e.,bytes)
Control (C)	- 8 or 16 bits
Data	- Variable
Frame Check Sequence (FCS)	- 16 or 32 bits
Flag (F)	- 8 bits

The flag, address and control fields that precede the data field are known as a header. The FCS and flag fields following the data field are referred to as a trailer.

The flag fields delimit the frame at both ends with the unique pattern 01111110. A single flag may be used as the closing flag for one frame and the opening flag for the next. All active stations attached to a link are continuously hunting for the flag sequence to synchronize on the start of a frame. While receiving a frame, a station continues to hunt for that sequence to determine the end of the frame, as the frames are not of uniform length. However, because the HDLC frame allows arbitrary bit patterns, there is no assurance that the pattern 01111110 will not appear somewhere inside the frame, thus destroying frame-level synchronization. To avoid this problem, a procedure known as bit stuffing is used. The transmitter will always insert an extra 0 bit

after each occurrence of five 1's in the frame (with the exception of the flag fields). After detecting a starting flag, the receiver monitors the bit stream. When a pattern of five 1's appears, the sixth bit is examined. If this bit is 0, it is deleted. If the sixth bit is a 1 and the seventh bit is a 0, the combination is accepted as a flag. If the sixth and seventh bits are both 1, the sending station is signaling an abort condition.

The frame check sequence is applied to the remaining bits of the frame, exclusive of flags. The normal FCS is the 16-bit CRC-CCITT standard. An optional 32-bit FCS, using CRC-32, may be employed if the frame length or line reliability dictates this choice. For purposes of illustration, only the 16-bit FCS is considered herein.

The purpose of each frame check sequence (FCS) is to allow the detection by the receiver of any errors that may have occurred during the transmission of a frame. The FCS consists of 16 bits of parity checking information that is computed at the sending side, prior to bit stuffing, from the bits contained in the address, control, and data fields, if present.

The computational procedure is derived from the well-known theory of cyclic codes. It proceeds as follows: Let the k binary bits contained in the address, control, and data fields of the frame by denoted by

$$a_{k-1}, a_{k-2}, \ldots, a_1, a_0$$

and represented algebraically by the binary polynomial

$$G(x) = a_{k-1}x^{k-1}+a_{k-2}x^{k-2}+\ldots+a_1x+a_0$$

where a_{k-1} is the first bit following the opening flag. Also define an auxiliary polynomial

$$L(x) = x^{15}+x^{14}+\ldots+x^{+1}$$

and the generator polynomial

$$P(x) = x^{16}+x^{12}+x^5+1$$

The polynomial P(x) has been standardized by the CCITT in Recommendation V.41 for use on general user-to-network interfaces.

Compute the remainder polynomial of the modulo-2 division of the polynomial

$$x^{16}G(x)+x^kL(x)$$

by P(x) and denote this remainder by

$$R(x) = r_{15}x^{15}+r_{14}x^{14}+\ldots+r_1x+r_0$$

The frame check sequence is the ones complement of the coefficients of R(x) and is represented by the polynomial

$$FCS=R(x)+L(x)$$

The complete frame of n=k+16 bits exclusive of the beginning and ending flags then takes the form

$$M(x)=x^{16}G(x)+R(X)+L(X)$$

The division by the generator polynomial is performed on the data sequence that has been modified in two ways. First the multiplication of G(x) by the factor x^{16} is equivalent to appending 16 zeroes to the sequence and creates the space for the FCS in the frame. Second, the addition of $x^kL(x)$ to $x^{16}G(x)$ corresponds to the inversion of the first 16 bits of the data sequence

and provides protection against the obliteration of the opening flag.

During transmission, the message M(x) may incur errors through the deletion or addition of bits or a change in their logical value. The latter type of error can be represented by the addition of the polynomial

$$E(x) = e_{n-1}x^{n-1}+e_{n-2}x^{n-2}+\ldots+e_1x+e_0$$

to the message, so that the received message is given by

$$M_r(x)=M(x)+E(x)$$

The receiver calculates the remainder $R_r(x)$ obtained by dividing the polynomial

$$x^{16}M_r(x)+x^nL(x)=x^{16}[x^{16}G(x)+x^kL(x)+R(x)]+x^{16}E(x)+x^{16}L(x)$$

by the generator polynomial P(x).

Given the relationship between G(x),R(x), and L(x) imposed at the sending end, the term in square brackets is evenly divisible by P(x). The desired remainder is therefore equal to the remainder that would be obtained from the division of

$$x^{16}E(x)+x^{16}L(x)$$

by P(x). This shows that $R_r(x)$ does not depend on the particular data sequence but is a function of the error pattern alone.

Now suppose that the message is received without errors of any kind. Then E(x)=0, and the preceding division results in the remainder

$$R_r(x)=x^{12}+x^{11}+x^{10}+x^8+x^3+x^2+x^1+1$$

Any other value of $R_r(x)$ therefore indicates the presence of errors in the received message.

A circuit 10 for a shift register implementation of the FCS calculation at the transmitter and receiver is shown in FIG 2. The circuit 10 comprises a shift register 13 formed from the storage elements 12 and gates 9.

The addition of $x^k L(x)$ to $x^{16}G(x)$ is accomplished by presetting the storage elements 12 of shift register 13 to binary 1. The register 13 calculates R(x) by enabling gates G2 and G3 and disabling via invertor 16 gate G1 using the input A. The k coefficients of G(x) arrive at the input 14 and are cycled through the register 13 via the feedback path through the gate 15 and the gate G3. At the same time the arriving data at the input 14 are shifted into the outgoing channel 25 via the gate G2 and gate 22. After k shifts, the register 13 contains the sixteen coefficients of R(x), which are then shifted into the channel 25 by enabling gate G1 and disabling gates G2 and gate G3. The inversion of the coefficients takes place in the inverter 27.

The register at the receiver, which is almost identical to the one at the transmitter, is again preset to binary 1. The entire received message $M_r(x)$ is then shifted through the register by enabling gates G2 and G3 and disabling gate G1. If the message contained no errors, the content of the register after n shifts will be the pattern

0 0 0 1 1 1 0 1 0 0 0 0 1 1 1 1

Any other error pattern would, of course, indicate the presence of one or more errors in $M_r(x)$.

The address field and control field are not of particular relevance to the present invention and are not discussed in detail herein.

Some devices connect two lines of different rates. For example, a concentrator may be collect data from many low rate terminals and place this data on a high speed transmission link connecting a host. An adapter may transform a HDLC-based protocol to another HDLC-based protocol.

FIG 3 illustrates a system 50 in which two transmission lines with different transmission rates are connected. An external device (not shown) transmits data to device D1 on line L0. The external device may be a conventional slow rate interface such as an RS-232. Device D1 is a transceiver which receives data on the line L0 and generates HDLC-like frames which are transmitted at a low rate on the line L1, which is a low bit rate line. Device D2 is an adapter or rate converter for adapting the HDLC-like frames on line L1 to appropriate HDLC-like frames which will be transmitted at a higher rate on the high bit rate line L2.

When there are data transmitted from high bit-rate line L2 to low bit-rate line L1, the adapter can transmit each data frame as soon as it is received. The data arrives much faster than it leaves. The transmitter of the adapter will not encounter underflow.

The adapter D2 may have a problem of overflow which can be solved by enlarging the size of the receiving buffer. In the reverse procedure, if the data frames are transmitted from the low-rate line L1 to the high-rate line L2, the transmitter of the adapter will have the possibility of data underflow.

Store-and-forward is the simplest method to solve this rate adaption problem. In accordance with the store-and-forward technique, the adapter or concentrator starts transmitting a data frame on the high bit rate line L2 after it receives the complete data frame from the low bit rate line L1. It first stores the whole frame in a receiving buffer. Then, the data frame is transmitted out over the high bit rate line. Under such scheme, there will be no possibility of underflow. However, the store-and-forward method has a shortcoming of having a long delay before a frame is transmitted via the high bit rate line.

A further problem with the store-and-forward technique is that the adapter D2 requires an FCS circuit, which as shown in FIG 2 comprises a shift register and associated logic. The adapter D2 also requires bit stuffing circuitry. These circuits add to the complexity and cost of the adapter.

The problem of rate adaption may be important in certain kinds of ISDN networks. ISDN is a general purpose digital network capable of supporting access to a wide range of interconnected services such as voice, data facsimile and video. ISDN achieves the support of

a large variety of services by providing a standard digital user-network interface. A standard network-user interface 60 is illustrated in FIG 4. A public network circuit 62 (e.g., a central office switch or PABX) is connected by a trunk line 63 to the fractional network termination unit (F-NT) 65. Illustratively, the trunk line 63 has a rate of 64 kbps. A plurality of terminal equipment 68 (TE's and F-TE's) are connected via S/T buses 67a, 67b to the network termination unit 65. Some of the terminal equipment is fractional (F-TE) and transmits at a rate of 64/N kbps where N is an integer greater than 2. The remainder of the terminal equipment (TE) is standard and transmits at 64 kbps. The physical frames transmitted on the S-bus from the terminal equipment to the network termination unit 65 comprise two B channels and one D channel (see, e.g., U.S. patent 4,920,723). Illustratively, the terminal equipment generates HDLC frames which are transmitted in a B or sub-B channel of the physical frames. Rate adaptation is necessary at the network termination unit 65 of FIG 4 to convert between the 64/N kbps bit stream transmitted on bus 67b and the 64 kpbs bit stream on the line 63.

In view of the foregoing it is an object of the present invention to provide a rate adapter and rate adaptation technique which receives frames such as HDLC frames on a low bit rate line and retransmits the frames on a high bit rate line with a minimum of delay. More specifically, it is an object of the present invention to provide a rate adapter and rate adaptation technique

which overcomes the shortcomings of the store-and-forward technique described above. It is a further object of the invention to provide an adapter and adaptation technique which requires neither an FCS circuit nor a bit stuffing circuit. It is also an object of the present invention to provide an adaptation technique for use at a fractional NT in an ISDN network.

Summary of the Invention

In a preferred embodiment, the present invention provides a rate conversion adapter which connects a first low bit rate transmission line and a second high bit rate transmission line. The adapter receives frames transmitted via the low bit rate line and retransmits these frames out over the high bit rate line with a minimum of delay.

The frames are of variable length and include a flag, an address field, a control field, a variable length data field, and a frame check sequence. Each frame arriving at the adapter over the low bit rate line also includes a length code indicative of the frame length, which length code does not alter a frame check sequence of the frame. In other words, the length code is divisible by a generator polynomial of the frame check sequence. The length code may follow the opening flag of a frame. Illustratively, the frames arriving at the adapter are HDLC frames which have been modified in accordance with the present invention to include the length code.

The adapter includes a processor which determines for each frame in response to its length code a specific time at which the adapter begins transmitting the frame out onto the high bit rate transmission line. The specific time is chosen so that the completion of the transmitting of the frame out over the high bit rate line is substantially simultaneous with the completion of the receiving of the frame from the low bit rate line. This eliminates the delays associated with the conventional store-and forward technique. The length code is removed from each frame before it is retransmitted out over the high bit rate line.

The adapter according to the invention requires neither an FCS circuit nor a bit stuffing circuit.

The inventive adapter is especially useful in certain kinds of ISDN networks. For example, a fractional terminal equipment (F-TE) may generate the frames with the length codes and transmit the frames in a sub-B channel at a rate 64/N kbps. The adapter forms part of a fractional network terminator (F-NT) which receives the frames at 64/N kbps and retransmits the frames at 64 kbps.

Brief Description of the Drawing

FIG 1 illustrates a conventional HDLC-like frame.

FIG 2 illustrates a circuit for performing a frame check sequence calculation.

FIG 3 schematically illustrates a system including a rate adapter.

FIG 4 schematically illustrates an ISDN network-user interface.

FIG 5 illustrates a modified HDLC-like frame according to the invention.

FIGs 6A, 6B, 6C, 6D and 6E together show a length code table storing length codes for use in frames in accordance with the present invention.

FIG 7 illustrates a device for generating modified HDLC-like frames in accordance with the invention.

FIG 8 illustrates an implementation of a rate adapter in accordance with the invention.

FIG 9 is a timing diagram which shows how the adaptation technique of the present invention reduces delays.

FIG 10 illustrates a user interface of an ISDN network which incorporates a rate adapter in accordance with the present invention.

Detailed Description of the Invention

In accordance with the present invention, the device D1 of FIG 3 generates modified HDLC frames rather than conventional HDLC frames. The modified HDLC frames are transmitted on the low rate line L1, received at the adapter D2, and retransmitted on the high rate line L2 with minimum delay. The modified HDLC frames include a length field which contains a length code illustratively comprising three bytes. A modified HDLC frame is illustrated in FIG 5. Note that the length field containing the length code immediately follows the

opening flag. The length code indicates the data length in the data field of the modified HDLC frame and does not change the FCS of the original (i.e., unmodified) HDLC frame. This eliminates the FCS calculation circuit at the adapter D2 of FIG 3. Furthermore, the length code avoids the bit stuffing procedure. This eliminates any need for a zero deletion and zero insertion circuit in the adapter D2 of FIG 3.

The following describes the coding methodology utilized in connection with the length code.

Referring to FIG 3, assume the following conditions:

(1) the L1 side transmission rate is 64/N(N=2,3,4,..) kbps

(2) the L2 side transmission rate is 64 kbps

(3) M represents the total bytes of a frame sent by D1

(4) M'=M-3 represents the total bytes of the frame sent by D2, as the three byte length code is removed before the adapter sends out the frames.

In accordance with the invention, when D2 receives X bytes from D1, then D2 start transmission so that D2 and D1 will complete transmission substantially concurrently. The transmission performance will be good with minimum time delay. The variable X is determined by the following equation:

$$(M-(X+3))*8/(64/N \text{ kbps}) = (M-3)*8/(64 \text{ kbps}) \qquad \text{(EQU-1)}$$

Solving EQU-1 for X, there is obtained

$$X=M*(N-1)/N+3*(N-1)N \qquad \text{(EQU-2)}$$

So, as long as the adapter D2 knows the whole length of the frame sent by D1, from EQU-2, the adapter D2 can calculate the right time to send the frame out onto L2.

The coding methodology for the length code of the Modified HDLC frame is to keep the FCS value unchanged when the length code is deleted and to avoid the bit stuffing procedure.

Refer again to FIG 2, the hardware implementation of the FCS circuit. At the beginning of a calculation, the shift register 13 is preset to all binary 1's. Then the bit stream from the address code is cycled through the shift register 13. If there is a data pattern which cycles through the register before the bit stream of the address field and which set the registers all to binary 1, then the presence of such a data pattern before the address field has no effect on the FCS value of the frame. The length codes used to modify the HDLC-like frames in accordance with the present invention have this property. Thus, the hardware circuity (see FIG 2) required for FCS calculation is not changed by the addition of the length code to the frame. Because the register number(i.e. number of bit locations in the shift register 13) is sixteen, the length code data pattern must exceed sixteen bits. So a twenty-four bit pattern to represent the length code in the modified HDLC frame is selected. Viewed another way, it may be

stated that the length code of a frame is divisible by a generator polynomial of the FCS.

Utilizing the foregoing and using software (C language) to model the FCS hardware in FIG 2, there is obtained the coding table of FIGs 6A, 6B, 6C, 6D and 6E. In the coding table, there is a total 256 three byte data patterns which can set the registers to binary 1, but only 180 data patterns which do not have five 1's continuous in the data pattern. Note the first byte in every data pattern is different and the numerical value is equal to 0 to 255. We use the first byte value to represent the data length of the frame. If a length code has five consecutive 1's, the next length code without five consecutive 1's is utilized. For example, if the data length is 22, because the length code for 22 had five consecutive 1's then there is used the length code corresponding to 24 to replace the length code corresponding to 22 to indicate the data length. This enlarges the original data length.

In the above-mentioned coding table, the maximum data length value of available length codes is 246. If there is a need to utilize data lengths greater than 246, the corresponding length code can be multiplied by 2 to indicate a data length greater than 246. However, with this method, the accuracy of the data length will be effected and the transmission performance will be decreased. Alternatively, in order to obtain better performance and accuracy, the length field may be increased to 32 bits (4 bytes). In this alternative

approach, the same, foregoing methodology is utilized to obtain a new coding table.

The whole operation carried out by the system 50 of FIG 3 according to the invention can be described as following:

* D1 receives data from L0 and decides the data length of a frame to send to D2
* D1 gets the length code from a coding table and puts the length code in the length field of a modified HDLC frame
* D1 sends the modified HDLC frame to D2 via L1
* D2 receives the modified HDLC frame and extracts the length code
* D2 calculates the X value using EQU-2 and discards the length code
* D2 continues to receive the modified HDLC frame via L1 and puts the arriving bit stream in a FIFO
* When D2 receives X bytes it starts to transmit data in the FIFO out onto L2
* The frames transmitted on L2 are HDLC-like because the length code contained in the modified frames has now been removed.

Referring now to FIG 7, there is shown a block diagram of D1 for generating modified HDLC-like frames in accordance with the invention. The data come from L0 and are received by the First-In-First-Out buffer unit (FIFO) 111. The data length of the modified HDLC frame

to be generated is determined by the Length Count unit (LC) 114. The Look-up Table (LUT) 115, which can be implemented with Read Only Memory (ROM), stores the coding table. The buffer unit (BUF) 112 inserts the length field ahead of the data in the frame. The HDLC controller 113 packs the length field and data field to form a HDLC frame. Then the transmitter (TX) 116 transmits the modified frame out on the low bit rate line L1.

FIG 8 is a block diagram of an adapter D2 in accordance with the invention. The modified HDLC frames are received by the receiver (RX) 224 from low bit rate line L1. The delete length field unit (DLF) 221 discards the length field of each modified HDLC frame and puts the other data in the First-In-First-Out buffer (FIFO) 222 in order including the flag field. The calculate length field unit (CLF) 227 gets the length field and calculates the X value using EQU-2. The HDLC bytes count unit (HBC) 225 counts how many bytes have been received in the modified HDLC frame. The compare logic unit (CL) 226 compares the X value with the byte count in the modified HDLC frame maintained by the counter 225. When the byte count value equals X, the CL 226 will indicate to the transmitter (TX) 223 to start the transmitting the data in FIFO 222 out onto the high bit rate L2. In this manner, reception of the frame via L1 and transmission of the frame onto L2 are completed at substantially the same time by the adapter D2 in accordance with a preferred embodiment of the invention.

FIG 9 shows how the adapter of the present invention reduces or eliminates delays characteristic of the prior art store-and-forward technique. At time t1, a frame comprising M bytes is received at the adapter D2 via the low bit rate line L1. At time t2, when X bytes have been received at the adapter, the adapter begins to transmit out on the high bit rate line L1. At time t3, both receiving of the frame via L1 and transmission of the frame via L2 are completed by the adapter. It should be noted that the frame arrives at the adapter containing M bytes. However, because the length code is removed, the frame leaves the adapter with M'=M-3 bytes. On the other hand, using the prior art store-and-forward technique, transmission would not begin until after reception is complete so that transmission would not be complete until time t4.

An alternative embodiment of the invention is illustrated in FIG 10. The embodiment of the invention shown is applicable to an ISDN network. More specifically, FIG 10 shows a user interface 200. The user 200 interface includes a fractional terminal equipment (F-TE) 300 and a fractional network terminator (F-NT) 400.

The F-TE 300 serves for generating modified HDLC frames in accordance with the invention. Thus, the F-TE 300 includes a ROM table 302 for storing a length code for each possible length of the modified HDLC frames. As discussed above, each length code is three bytes to insure that the length code does not alter the FCS value

of a frame, but the actual length is indicated by the first byte of the three byte length code.

The F-TE 300 also includes the R-Interface buffer 305, the HDLC transceiver 307, and the S-bus transceiver 309. The ROM table 302, Interface buffer 305, HDLC transceiver 307 and S-bus transceiver 309 are controlled by the CPU 311.

Data is received at the F-TE 300 via the input terminal 304 at a slow rate from an RS 232 interface, for example. The data is stored in the interface buffer 305. The HDLC transceiver 307 organizes this data into modified HDLC frames including a three byte length code which is retrieved from the ROM table 302. As indicated above, it is the first byte of the length code which codes the length and the last two bytes which insure that the length code is divisible by the FCS generator polynomial. The S-bus transceiver 309 puts the modified HDLC frames in a sub-B channel of an ISDN frame for transmission over the bus 313 at a rate of 64/N (N 2) kbps.

The frames are received at the F-NT 400 at the S-bus transceiver 402. The transceiver logic 404 removes the HDLC frames from the ISDN sub-B channel and places the first byte of the length code in the length buffer 406. The interrupt controller 408 interrupts the CPU 410 to read the length buffer 406 to determine M (i.e., number of bytes in the frame). The CPU then determines from EQU-2 when to start transmitting the frame, and puts the value X in the counter 412.

The second and third bytes of the length code of the HDLC-like frames are discarded and each byte of the arriving frame is written into the eight-bit-wide FIFO 407.

Each time a byte is written into the FIFO 407, the counter 412 discremented one count. In other words, each time a byte is received at the F-NT 400, the counter 412 is decremented one count. When the counter 412 reads zero, the S-bus transceiver 414 starts transmitting the frame from the FIFO 407 out onto the bus 416 at 64 kbps. As the length code has been discarded, the frame now has a conventional HDLC format.

It should be noted that in an illustrative embodiment of the invention the frames transmitted on the bus 416 satisfy the V.120 protocol. The frames on the bus 313 are modified to include the length code but otherwise conform to the V.120 protocol.

Finally, the above-described embodiments of the invention are intended to be illustrative only. Numerous alternative embodiments may be devised by those skilled in the art without departing from the spirit and scope of the following claims.

CLAIMS

1. An adapter for connecting a first transmission means which operates at a low transmission rate to a second transmission means which operates at a fast transmission rate comprising

receiving means for receiving frames transmitted on the first transmission means, each frame transmitted on the first transmission means comprising a flag, an address field, a control field, a data field of variable length, and a frame check sequence, each frame further including a length code corresponding to its length, each frame having a frame check sequence which is unaltered by the addition of the length code to the frame,

means for removing the length code from each frame,

transmitting means for transmitting each frame on the second transmission means beginning at a specific time individually determined for each frame, and

processing means for determining in response to the length code contained in each frame the specific time for said transmitting means to begin transmitting the frame, said specific time being chosen such that completion of the transmitting of the frame by said transmitting means substantially coincides with completion of the receiving of the frame by said receiving means.

2. The adapter of claim 1 wherein the length code of

each frame is divisible by a generator polynomial of the frame check sequence.

3. The adapter of claim 2 wherein said adapter is part of an ISDN network.

4. The adapter of claim 3 wherein said adapter forms part of a fractional network terminator (F-NT) of said ISDN network.

5. The adapter of claim 4 wherein said adapter is connected via said first transmission means to a fractional terminal equipment (F-TE) of said ISDN network, said fractional terminal equipment generating said frames including said length code for transmission over said first transmission means.

6. The adapter of claim 1 wherein said adapter is connected via said first transmission means to a circuit for generating said frames comprising

means for receiving data,

means for storing a length code corresponding to each possible length of said frames,

means for formatting said data into said frames of variable length including means for retrieving from said storing means the length code corresponding to the length of each frame and inserting the length code into the frame.

7. An adapter for connecting a low transmission rate link to a fast transmission rate link comprising

means for receiving from the low transmission rate link frames of variable length including a length code and a frame check sequence, wherein the length code

of each frame is divisible by a generator polynomial of the frame check sequence of the frame, means for transmitting each frame onto the fast transmission rate link after removing the length code, and processing means for determining in response to the length code in each frame a specific time at which the transmitting means begins transmitting the frame onto the fast link such that the completion of the transmitting of the frame onto the fast link substantially coincides with the completion of the receiving of the frame from the low rate link.

8. The adapter of claim 7 wherein said adapter is connected via the low rate link to a device for generating said frames, said device comprising memory means for storing a length code corresponding to each possible frame length, means for formatting data into frames of variable length including means for retrieving for each frame the corresponding frame length code from said memory means and inserting the corresponding frame length code into each frame, and means for transmitting the frame onto said low rate transmission link.

9. The adapter of claim 8 wherein

said adapter is located in an ISDN network, and forms a fractional network termination (F-NT) unit of said ISDN network,

said low rate transmission link is formed by an ISDN bus and wherein said frames are transmitted via said bus in a B channel of ISDN interface frames, and

said device is a fractional terminal equipment (F-TE) of said ISDN network.

10. A method for interfacing first transmission means with a low transmission rate and a second transmission means with a high transmission rate comprising the steps of

generating frames of variable length, each frame including a length code indicative of the length of the frame which does not alter a frame check sequence value of the frame,

transmitting the frames via the first transmission means to an adapter,

receiving each frame transmitted via the first transmission means at said adapter, and after removing the length code, transmitting each frame onto the second transmission means beginning at a specific time such that the transmitting of the frame onto the second transmission means is complete at substantially the same time as the receiving of the frame via the first transmission means is complete.

11. The method of claim 10 wherein said generating step comprises maintaining a memory for storing a length code corresponding to each possible frame length and retrieving from said memory the length code for each frame and inserting the length code into the frame.

12. The method of claim 11 wherein said generating step takes place at a fractional terminal equipment of an ISDN network, wherein said first transmission means is formed by a bus, and wherein said frames are transmitted

over said first transmission means in an ISDN B channel to a fractional network terminator incorporating said adapter.

13. A method for transmitting data frames comprising the steps of

generating frames comprising a delimiting flag, a length code following the flag, an address field, a control field, a variable length data field, and a frame check sequence, said length code not altering the frame check sequence of a frame,

transmitting the frames via a first low bit rate transmission medium,

receiving the frames at an adapter, and

retransmitting the frames by the adapter out onto a second high bit rate transmission medium after removing the length code starting at a time determined in response to the length code for each frame such that the transmitting and retransmitting steps for each frame are completed substantially simultaneously.

14. Adapter for transmission lines using HDLC frames substantially as hereinbefore described with reference to the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

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Databases (see over)
(i) UK Patent Office

(ii)

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Documents considered relevant following a search in respect of claims 1-14

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

Category	Identity of document and relevant passages	Relevant to claim(s

Categories of documents

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